In the Specification

Please replace the paragraph beginning on page 8, line 22 and ending on page 8, line 33 with the following amended paragraph.

In typical implementations, the generator program 105 can identify the selections and generate a logic description with information for implementing the various modules. The generator program 105 can be a Perl script creating HDL files such as Verilog, Abel, VHDL, and AHDL files from the module information entered by a user. According to various embodiments, the generator program 105 also provides information to a synthesis tool 107 to allow HDL files to be automatically synthesized. In some examples, a logic description is provided directly by a designer. Some of the available synthesis tools are Leonardo Spectrum, available from Mentor Graphics Corporation of Wilsonville, Oregon and Synplify available from Synplicity Corporation of Sunnyvale, California. The HDL files may contain technology specific code readable only by a synthesis tool. The HDL files at this point may also be passed to a simulation tool[[109]].

Please replace the paragraph beginning on page 11, line 6 and ending on page 11, line 10 with the following amended paragraph.

Figure 2 is a diagrammatic representation showing more detailed processing associated with synthesis and simulation tools. According to various embodiments, an HDL design file such as a VHDL source file 201 is provided for both logic synthesis and simulation. The VHDL source file 201 may be provided to a ~~synthesis~~ timing analysis tool [[203]] 211, simulation ~~software 221~~ tool 213, and ~~simulation software 225~~ a synthesis tool 215.

Please replace the paragraph beginning on page 11, line 12 and ending on page 11, line 17 with the following amended paragraph.

The synthesis tool [[203]] 215 takes the VHDL source file 201 and generates output information such as an EDF ~~files files 211~~ input file 225 for implementing the design on an electronic device. It should be noted that the synthesis tool [[203]] 215 may also output other files such as assignment and configuration (ACF) files [[213]] 223, as well as project library mapping (LMF) files [[215]] 221. A variety of tools can be used to process available HDL design files.

Please replace the paragraph beginning on page 17, line 10 and ending on page 17, line 20 with the following amended paragraph.

Figure 8 is a process flow diagram showing one example of a technique for inserting randomized functionality and conductivity. At 803, the corresponding input is selected for each output. At 805, the probabilistic function is applied to determine how to drive the output. In some examples, output is directly wired to an input at 807. For example, the sub module input line may be directly wired to a top-level input pins. In another example, the top-level output pins can be directly wired to register. In still another example, the top-level output pins can be wired to a top-level input pin. A probabilistic function may also determine that each output should be driven using a logical expression operation and the corresponding input at 809. In another example, the output can be driven using a ~~mass knuckle~~ mathematical expression operation and the corresponding input at 811.

Please replace the paragraph beginning on page 17, line 30 and ending on page 18, line 5 with the following amended paragraph.

Figure 9 illustrates a typical computer system that can be used to implement a programmable chip in accordance with an embodiment of the present invention. The computer system 900 includes any number of processors 902 (also referred to as central processing units, or CPUs) that are coupled to devices including memory 906 (typically a random access memory, or "RAM"), memory 904 (typically a read only memory, or "ROM"). The processors 902 can be configured to generate a ~~testbeenh~~ testbench for a particular design automation tool. As is well known in the art, memory 904 acts to transfer data and instructions uni-directionally to the CPU and memory 906 is used typically to transfer data and instructions in a bi-directional manner.